

FIG.1

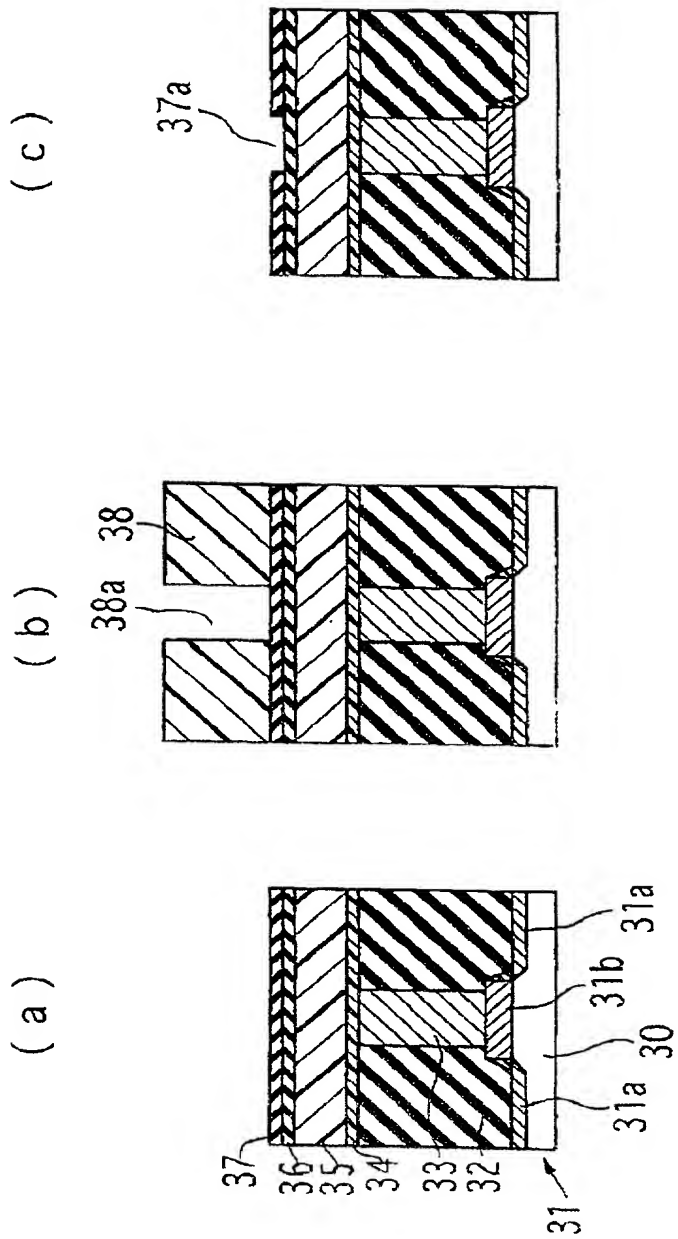


FIG.2

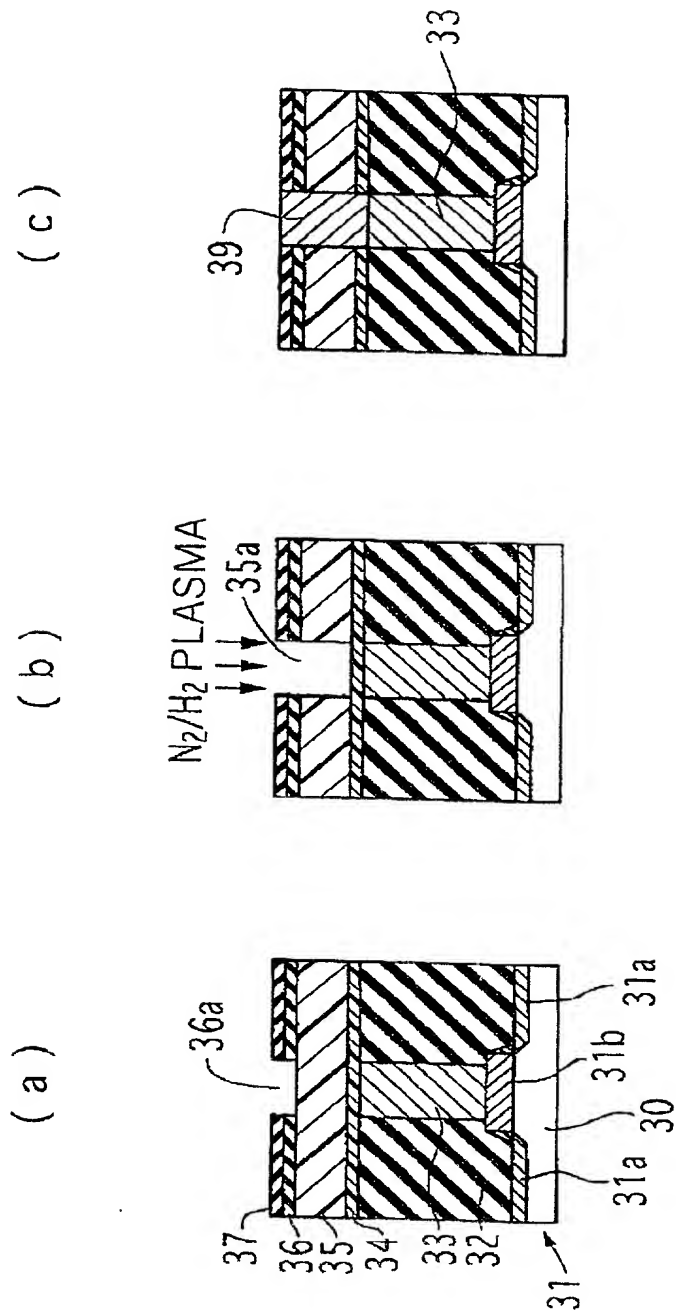


FIG.3

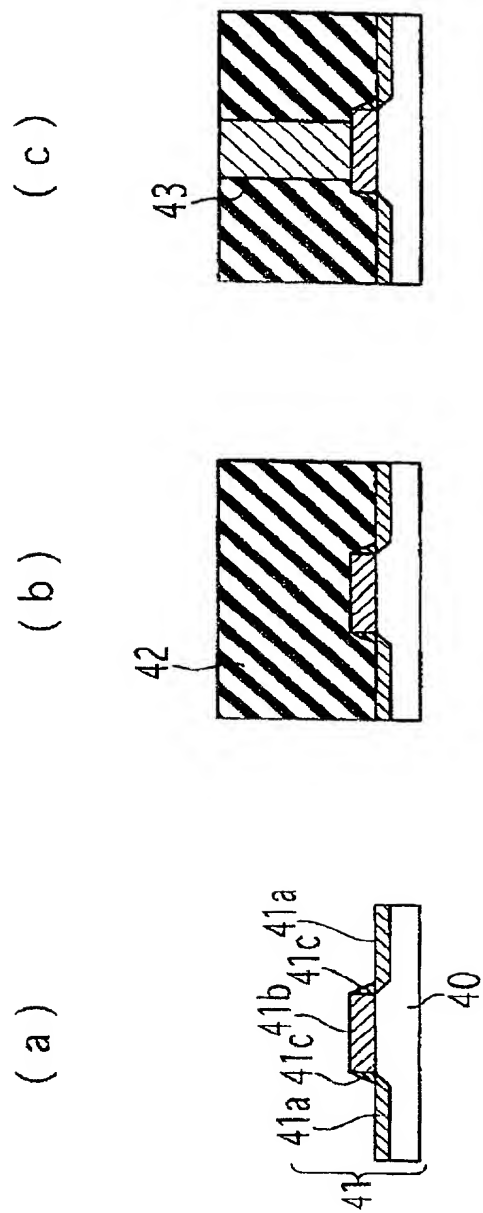


FIG. 4

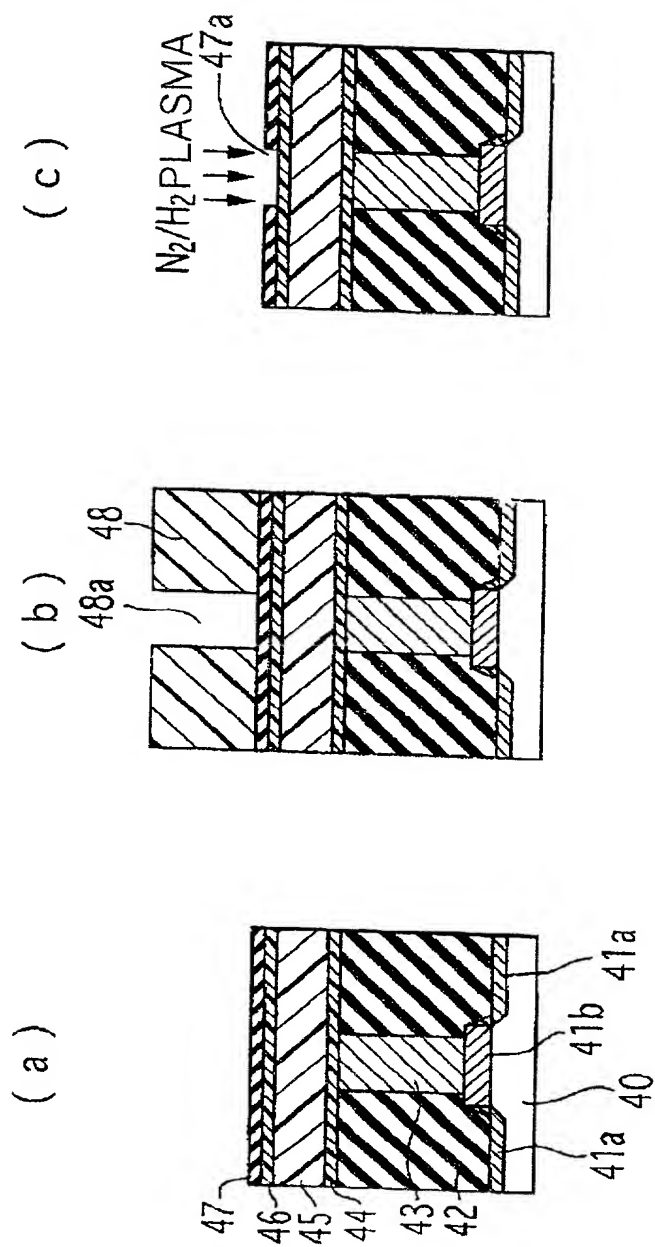
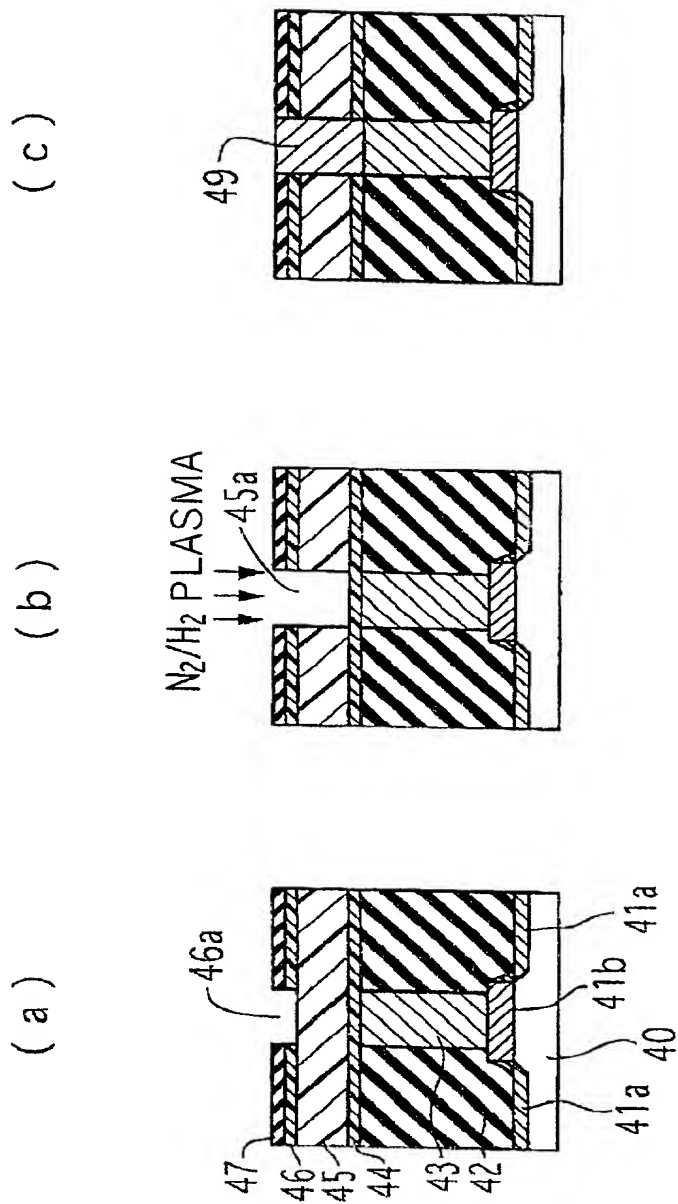


FIG. 5



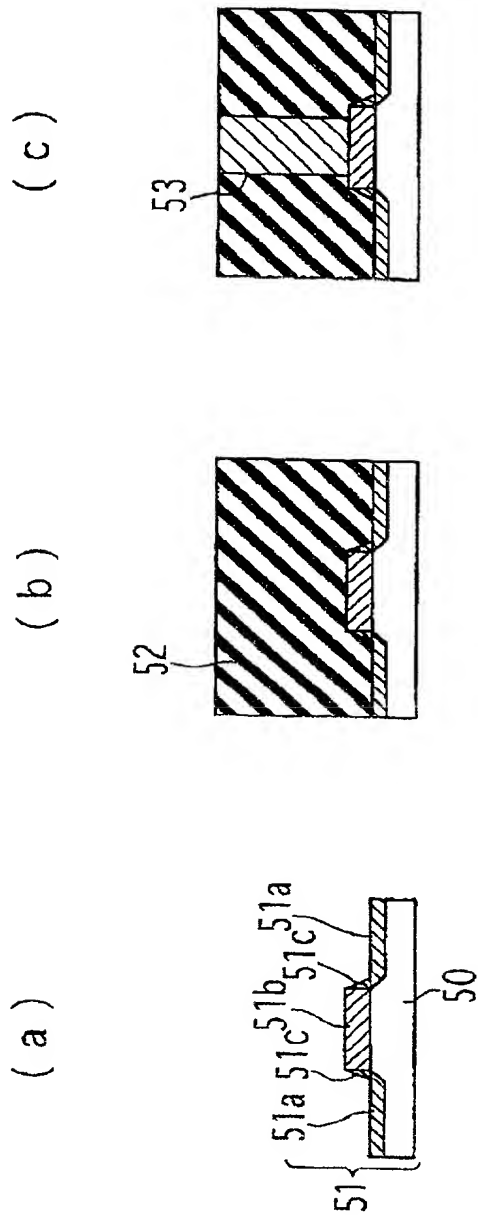


FIG. 7

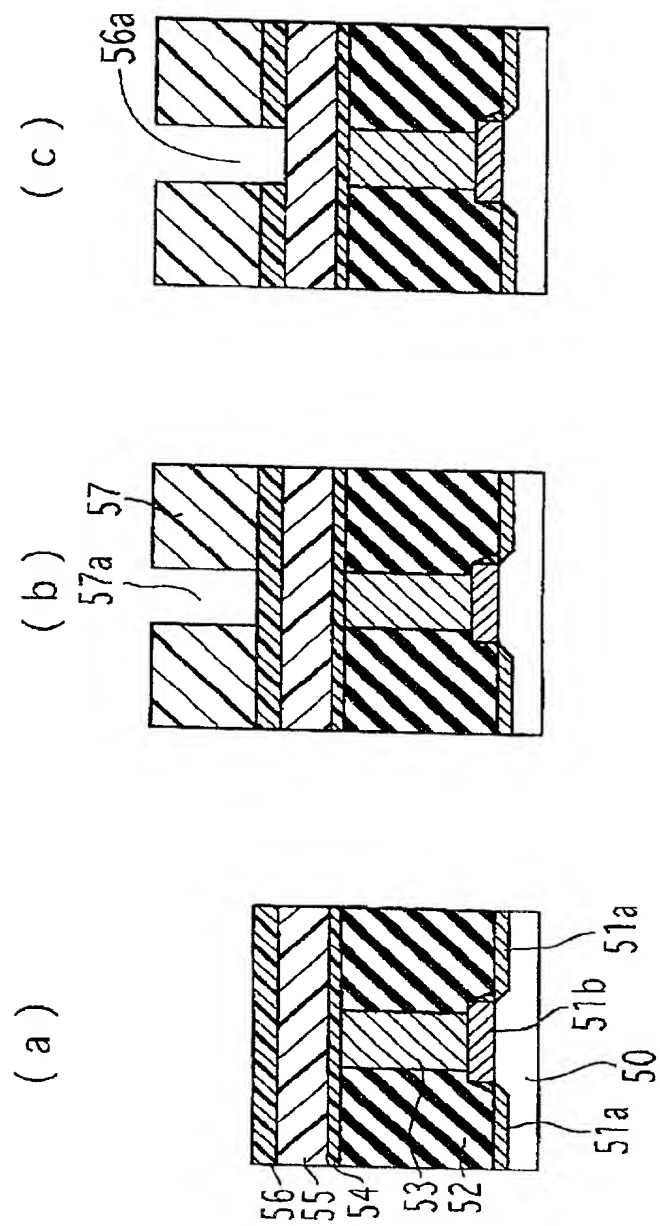


FIG. 8



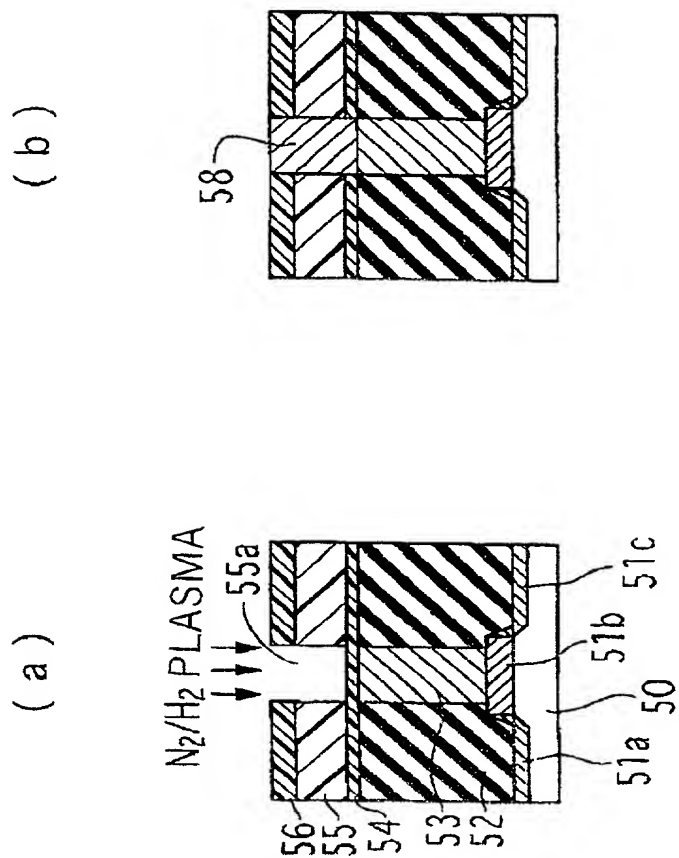
[illegible]

FIG. 9

FIG. 10 is a cross-sectional view of a semiconductor device in a third embodiment, showing a different structure from the first and second embodiments.

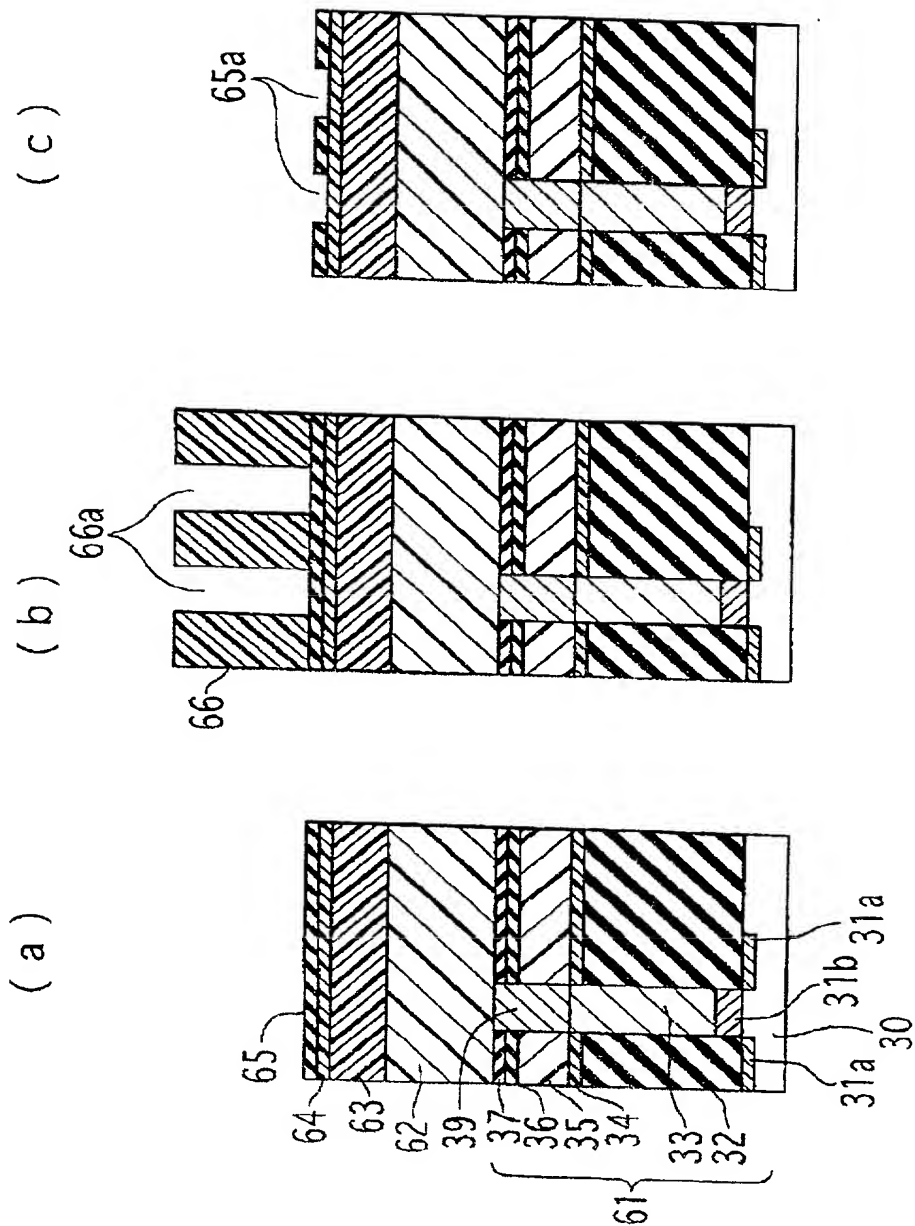


FIG.10

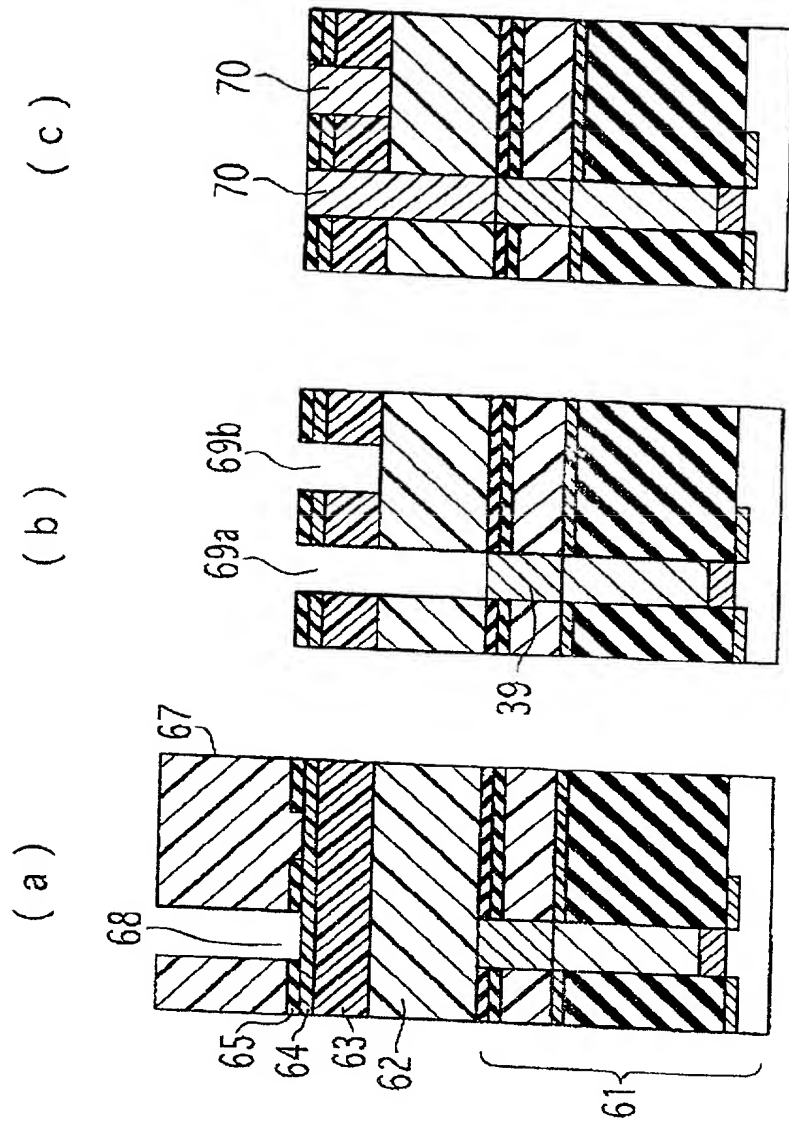


FIG.11

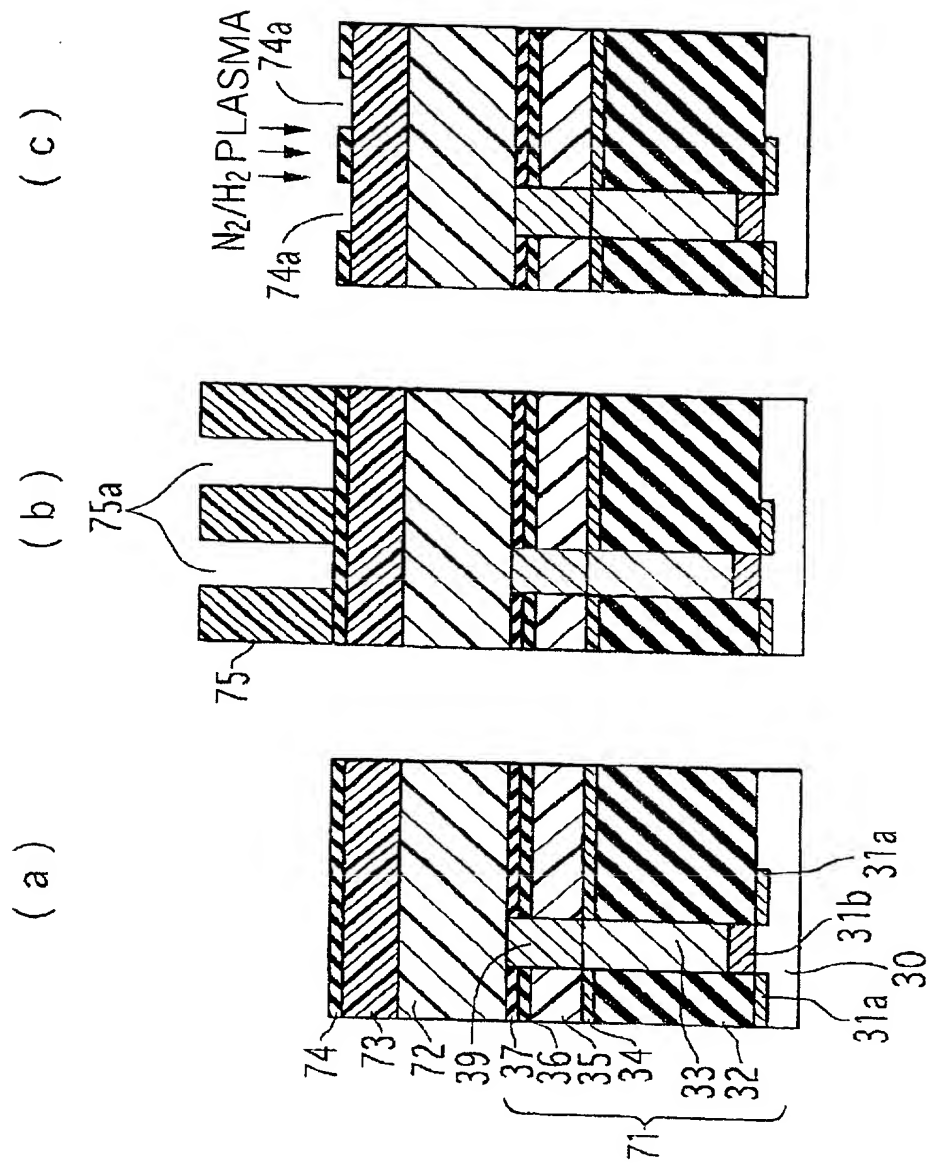


FIG.12

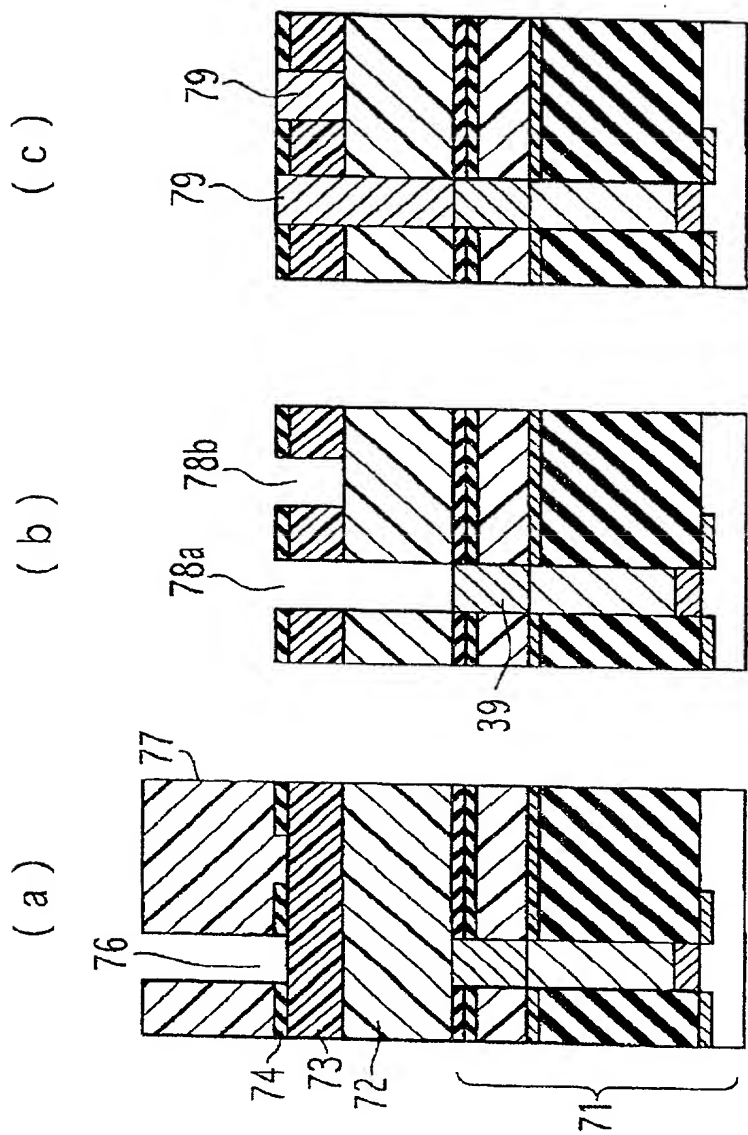


FIG. 13

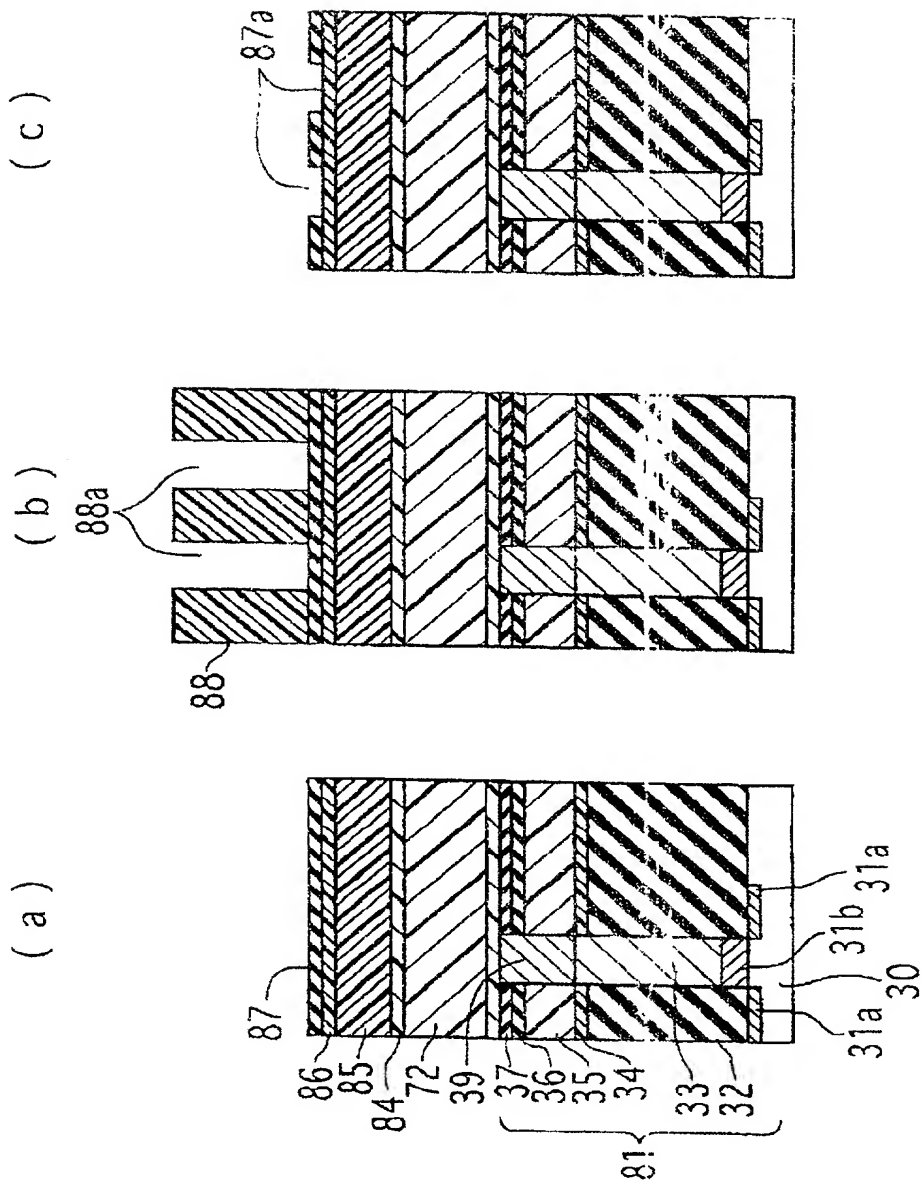


FIG.14

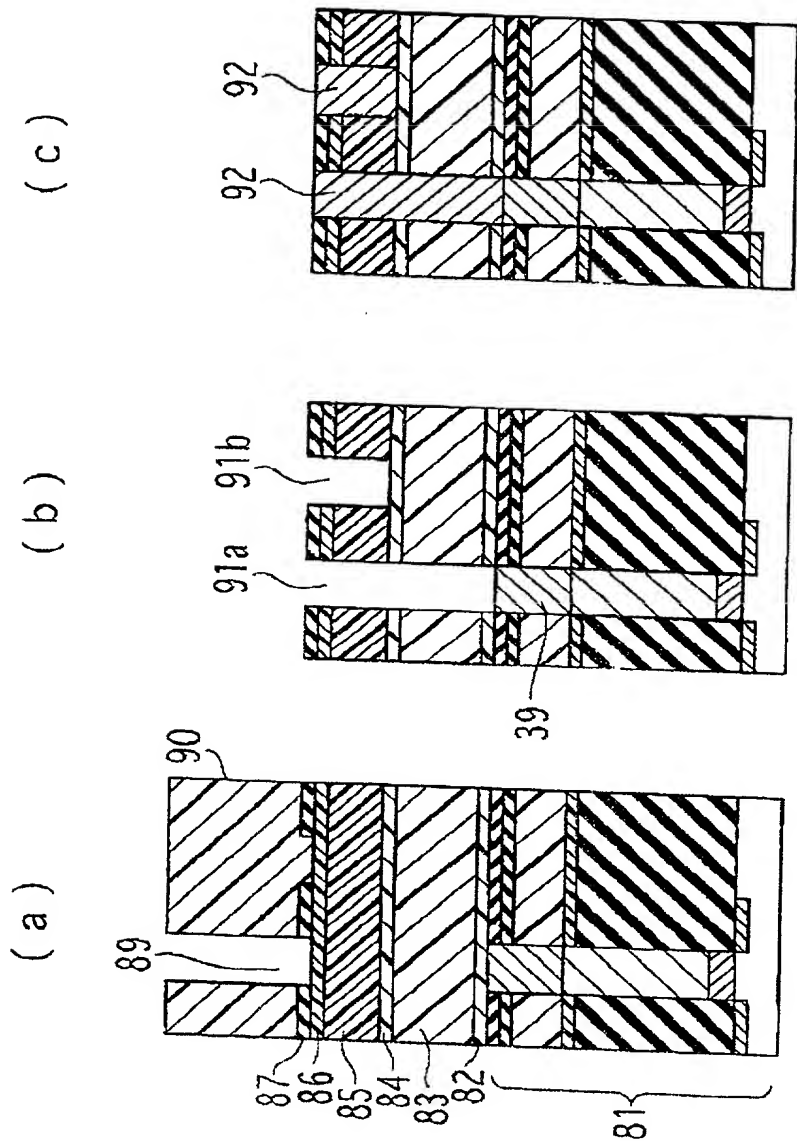


FIG.15

FIG. 16 is a cross-sectional view of a semiconductor device in a third state.

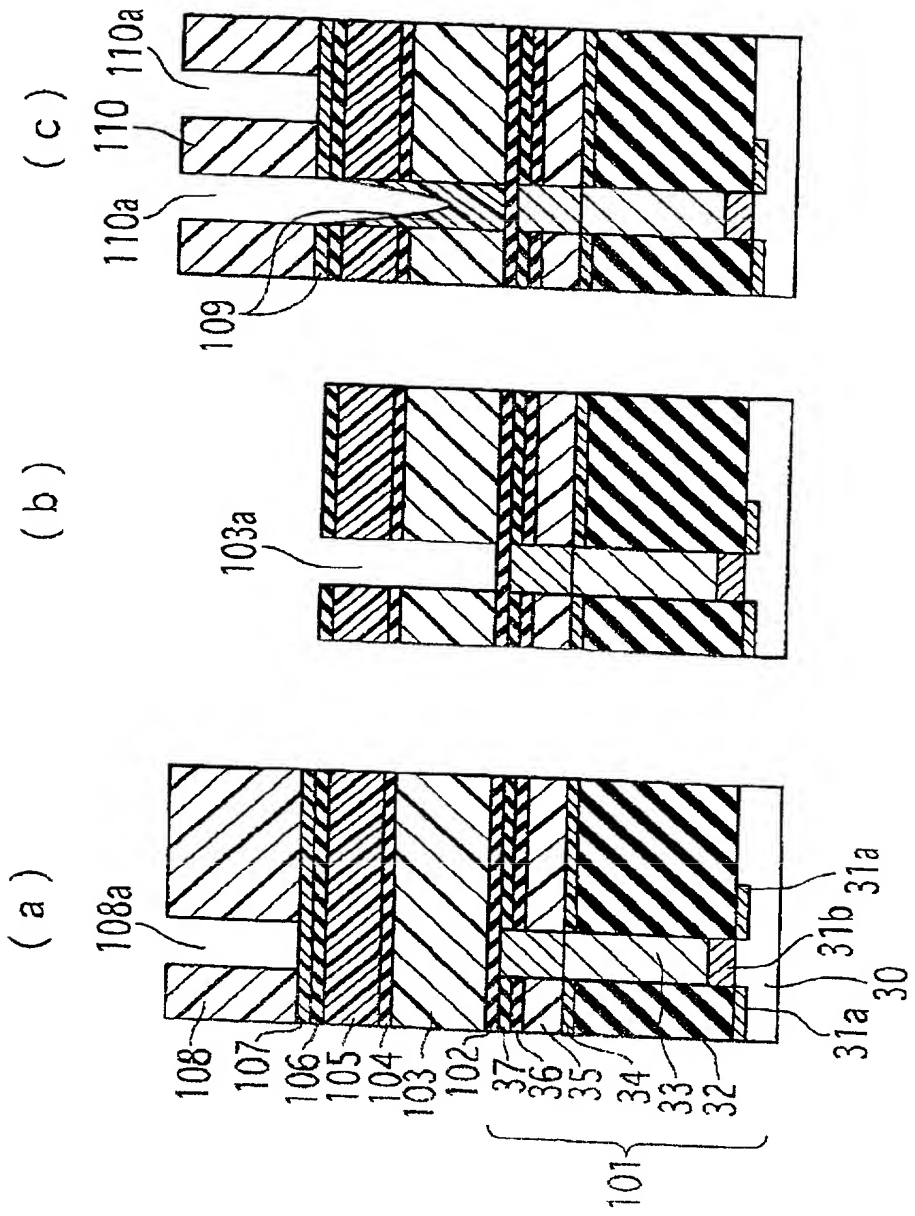


FIG.16



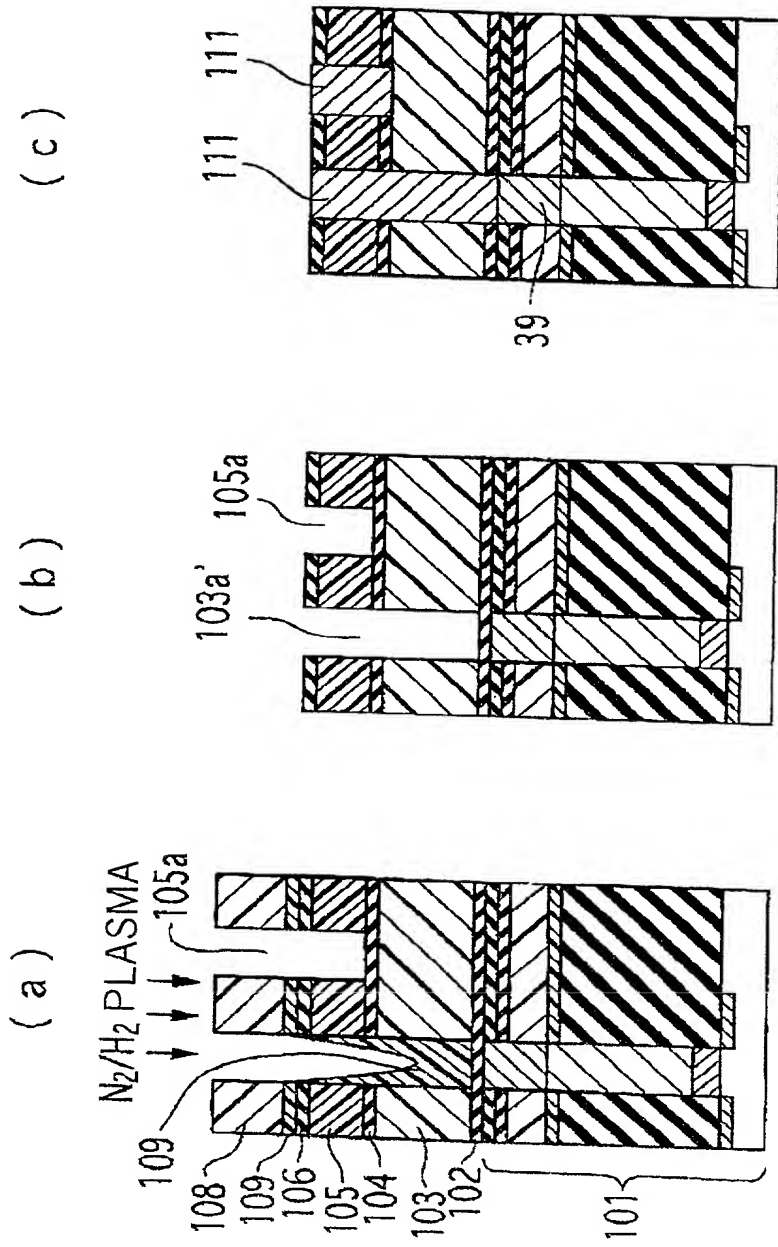


FIG.17



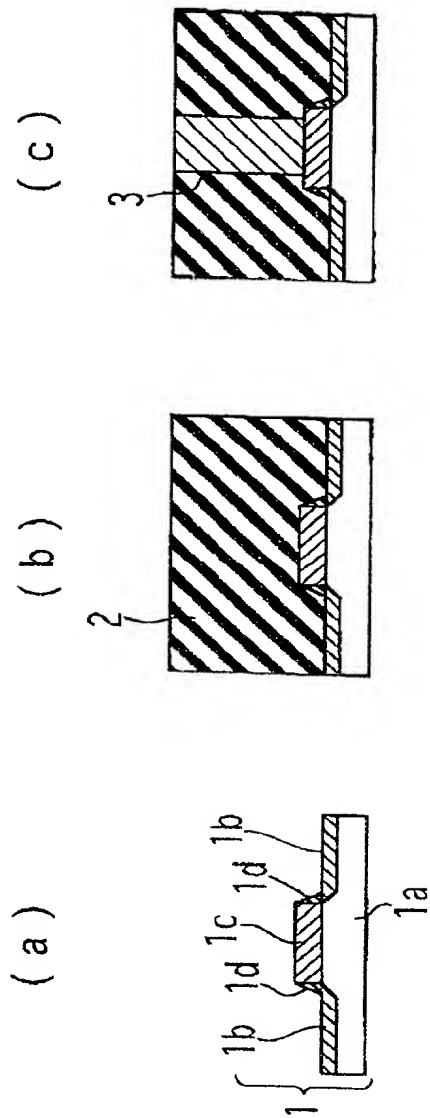


FIG. 19

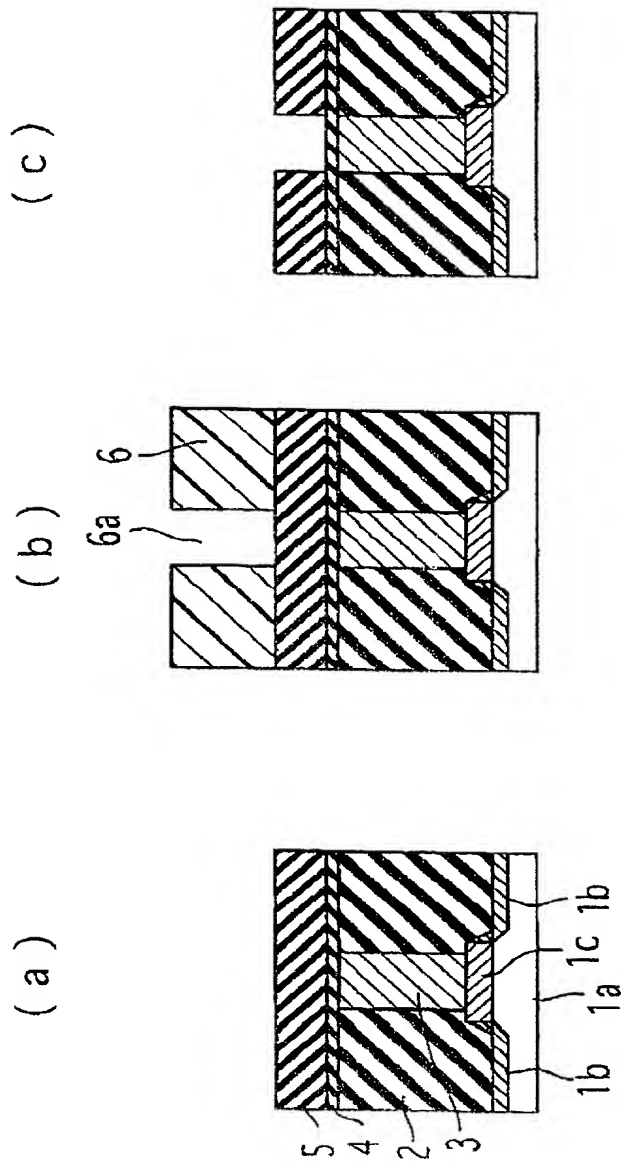


FIG.20



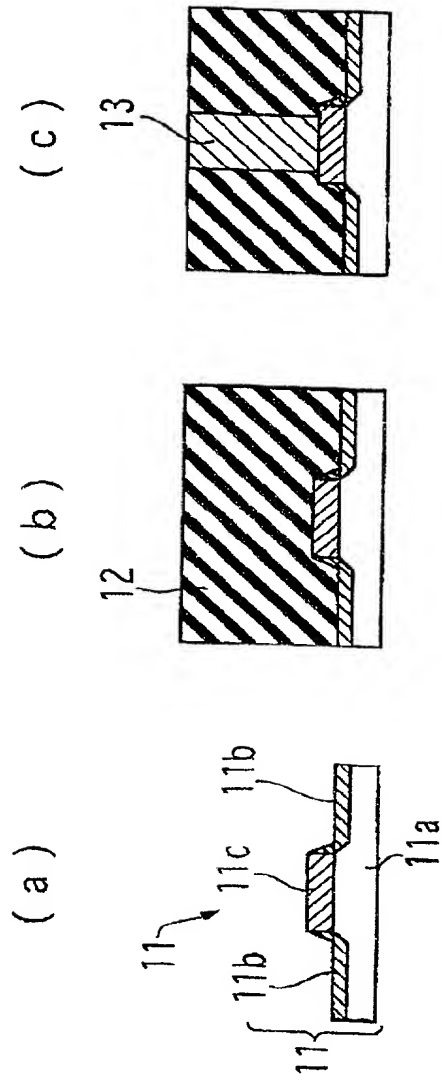


FIG. 22

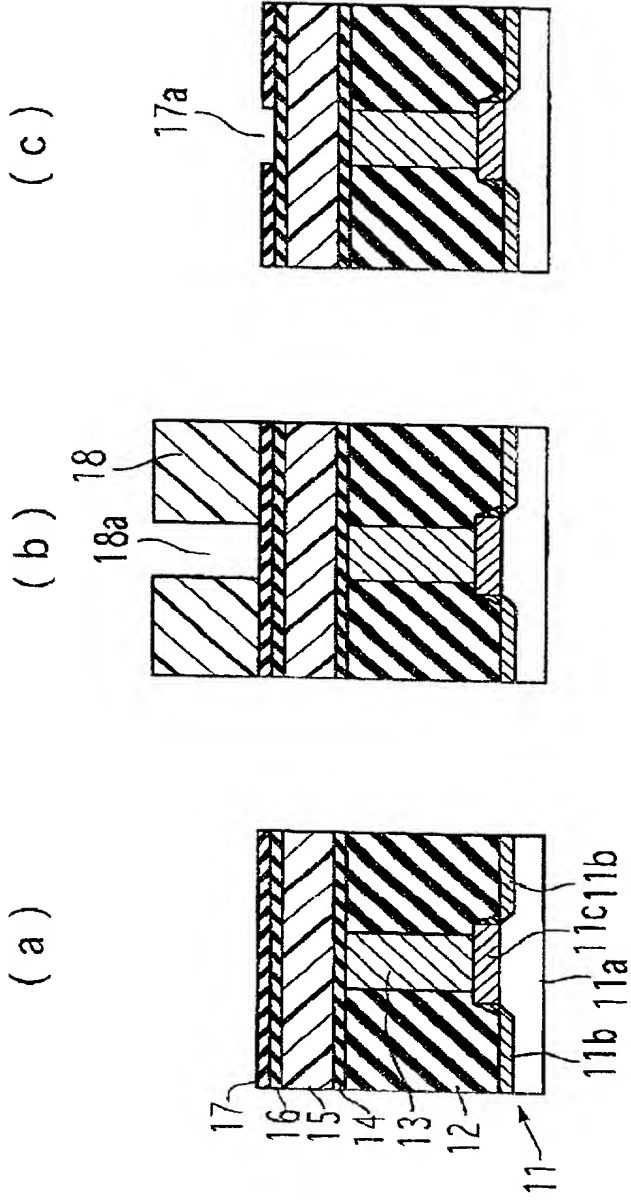


FIG. 23

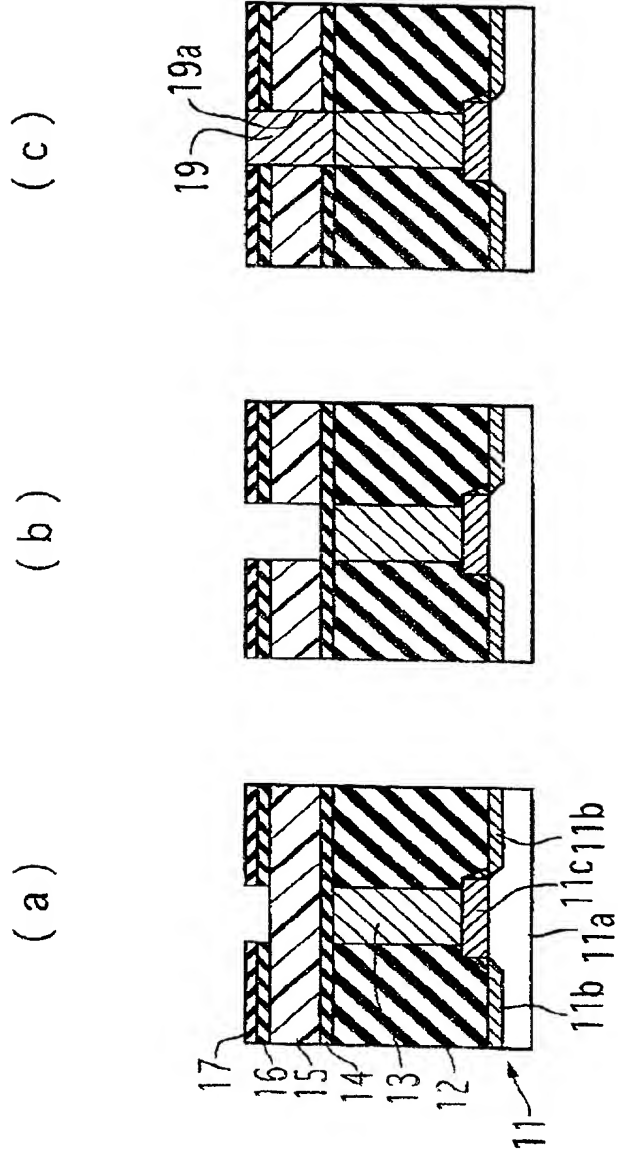


FIG.24



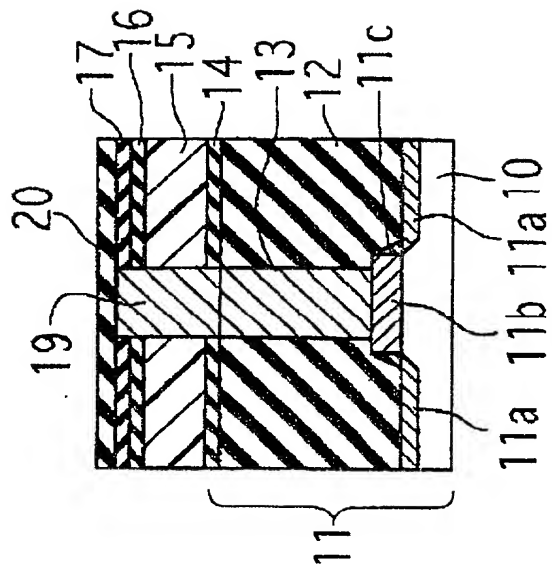


FIG.25